Remarks

Thorough examination by the Examiner is noted and appreciated.

Examiner has indicated that claims 1-20 are outstanding and that claims 1-20 are rejected.

The claims have been amended to clarify Applicants invention.

Support for the amended claims are found in the original claims and/or the Specification. No new matter has been added.

For example support for the amendments is found in the Specification paragraph 0031:

"By performing at least a plasma treatment, more preferably followed by an annealing treatment according to preferred embodiments, plasma implanted atoms such as hydrogen, nitrogen, and oxygen, more preferably hydrogen and/or nitrogen, penetrate and thermally diffuse to the HfO_2/polysilicon interface to passivate or bond with the dangling bonds. **As a result, interface states acting as electron/hole traps are advantageously reduced thereby improving flatband and consequently threshold Voltage behavior in both PMOS and NMOS**

devices."

Claim Rejections under 35 USC 103

1. Claims 1-7, 9, 11, and 12 stand rejected under 35 USC 102(e) as being anticipated by Park et al. (US 6,803,275).

Parker et al. disclose a process for forming a flash memory device including forming an ONO structure on a semiconductor substrate where the bottom oxide layer treated to reduce oxygen vacancies is to avoid charge leakage paths from the overlying charge storage layer(see Abstract; col 3, lines 15-21). Parker et al. disclose that the bottom oxide layer and the charge storage layer (N layer) may be a high-K dielectric (see Abstract; col 6, lines 12-19; col 14, lines 9-28; col 17, lines 17-35).

Prior to forming the charge storage dielectric on the bottom oxide layer **the entire bottom oxide layer** is treated under oxidizing conditions (col 13, lines 9-10; Figure 3; Figure 7), e.g., oxygen and inert gas plasma (col 11, lines 61 to col 12, line 59) to decrease an oxygen vacancy content of the bottom oxide layer. Parker et al. disclose that an annealing process in

an oxidizing atmosphere takes place following the oxidizing plasma treatment (col 12, lines 40-58). **Following formation and treatment of the ONO layer**, a gate electrode layer is formed on the top oxide layer and **then** patterned and etched to form a gate structure (col 19, lines 52-61).

Thus, Parker et al. disclose a significantly different process than Applicants and fail to disclose several aspects of Applicants disclosed and claimed invention.

Parker et al. fail to disclose:

"A method for treating a gate structure comprising a high-K gate dielectric stack to **reduce interface states between a high-K gate dielectric and a gate electrode**"

Parker et al. also fail to disclose Applicants process steps including:

"forming a gate electrode layer on the gate dielectric layer stack;

lithographically patterning and etching to form a gate structure; and,

carrying out at least one plasma treatment of the gate structure following formation of the gate structure following formation of the gate structure, said at least one plasma treatment comprising a plasma source gas selected from the group consisting of H_2, N_2, O_2, NH_3, and combinations thereof."

Thus, Parker et al. is clearly insufficient to anticipate Applicants disclosed and claimed invention.

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

"The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Claim Rejections under 35 USC 103

2. Claim 8 stands rejected under 35 USC 103(a) as being unpatentable over by Park et al., above, in view of Sarigiannis et al. (USPUB 2004/0152304).

Applicants reiterate the comments made above with respect to Park et al.

The fact that Sarigiannis et al. disclose an ALD deposition process where a purge time is decreased to remove active species of pre-cursor gases from reactors (paragraph 0010) does not further help Examiner in making out a *prima facie* case.

"Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).*

3. Claims 10, 13-18, and 20 stand rejected under 35 USC 103(a) as being unpatentable over by Park et al., above, in view of Baum et al. (USPUB 2002/0175393).

Applicants reiterate the comments made above with respect to Park et al.

The fact that Baum et al. disclose a CVD process for growing hafnium oxide films (see paragraph 0166 and Table II) does not further help Examiner in making out a *prima facie* case. Baum et al. nowhere disclose a plasma treatment as Applicants have disclosed and claimed.

"Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).*

3. Claim 19 stands rejected under 35 USC 103(a) as being unpatentable over by Park et al., and Baum et al., above and further in view of Possin et al. (5,281,546).

Applicants reiterate the comments made above with respect to Park et al. and Baum et al.

Even assuming *arguendo* a proper motivation for combination, the fact that Possin et al. disclose "A method of fabricating a thin film transistor (TFT) including the steps of forming a gate conductor on a substrate; depositing a gate dielectric layer over the gate conductor; depositing a layer of amorphous silicon over the gate dielectric layer; **treating the exposed surface of the amorphous silicon with a hydrogen plasma; depositing a layer of n+ doped silicon over the treated amorphous silicon surface** such that an interface is formed between the amorphous silicon and the n+ doped layer that has relatively low contact resistance" does not further help Examiner in making out a *prima facie* case.

"Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).*

"we do not pick and choose among the individual elements of assorted prior art references to recreate the claimed invention, but rather we look for some teaching or suggestion in the

references to support their use in a particular claimed combination". Symbol Technologies, Inc. v. Opticon, Inc., 935 F.2d 1569, 19 USPQ2d 1241 (Fed. Cir. 1991).

Conclusion

The cited reference, either individually, or in combination, fail to suggest or disclose Applicants disclosed and claimed invention, therefore failing to make out a prima facie case of obviousness with respect to Applicants independent claims, and therefore Applicants dependent claims.

Based on the foregoing, Applicants respectfully submit that the Claims are now in condition for allowance. Such favorable action by the Examiner at an early date is respectfully solicited.

In the event that the present invention as claimed is not in condition for allowance for any reason, the Examiner is respectfully invited to call the Applicants' representative at his Bloomfield Hills, Michigan office at (248) 540-4040 such that necessary action may be taken to place the application in a condition for allowance.

Respectfully submitted,

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